

What is claimed is:

1. A method for mounting multilayered ceramic capacitors on a circuit board having a front surface and a back surface, wherein each capacitor includes a body having dielectric layers formed of a dielectric ceramic material and internal electrode layers and a pair of external terminal electrodes formed on two sides of the body, the dielectric layers and the internal electrode layers being stacked alternately in the body and the internal electrode layers being connected in parallel to the external terminal electrodes in an alternate manner, the method comprising the steps of:

forming lands at substantially plane-symmetrical positions on the front and the back surfaces, wherein every two lands disposed at their substantially plane-symmetrical positions are connected each other; and

mounting the capacitors on the lands of the front and the back surfaces such that the external terminal electrodes of the capacitors are electrically coupled to the lands on the front and the back surfaces.

2. The method of claim 1, wherein said two lands are electrically coupled each other by a through hole formed therein.

3. A method for mounting multilayered ceramic capacitors on a circuit board having a front surface and a back surface, wherein each capacitor includes a body having dielectric layers formed of a dielectric ceramic material and internal electrode layers and a pair of external terminal electrodes formed on two sides of the body, the dielectric layers and the internal electrode layers being stacked alternately in the body and the internal electrode layers being connected in parallel to the external terminal electrodes in an alternate manner, the method comprising the step of:

mounting the capacitors on substantially plane-symmetrical positions of the front and the back surfaces, respectively, wherein the capacitors are substantially identical each other and substantially identical voltages are applied to the capacitors.

4. The method of claim 3, wherein said mounting step includes the steps of:

forming lands at substantially plane-symmetrical positions on the front and the back surfaces, wherein every two lands disposed at their substantially plane-symmetrical positions are connected each other; and

mounting the capacitors on the lands of the front and the back surfaces such that the external terminal electrodes of the capacitors are electrically coupled to the lands on the front and the back surfaces.

5. A method for mounting multilayered ceramic capacitors on a circuit board having a front and a back surfaces, the capacitors being used in an electronic circuit as components thereof and voltages applied to the capacitors being varied, wherein each capacitor includes a body having dielectric layers formed of a dielectric ceramic material and internal electrode layers and a pair of external terminal electrodes formed on two sides of the body, the dielectric layers and the internal electrode layers being stacked alternately in the body and the internal electrode layers being connected in parallel to the external terminal electrodes in an alternate manner, the method comprising the steps of:

forming lands at substantially plane-symmetrical positions on the front and the back surfaces, wherein every two lands disposed at their substantially plane-symmetrical positions are connected each other; and

mounting the capacitors on the lands of the front and the back surfaces such that the capacitors are disposed at substantially plane-symmetrical positions and the external terminal electrodes of the capacitors are electrically coupled to the lands on the front and the back surfaces, wherein the capacitors are substantially identical each other and substantially identical voltages are applied to the capacitors.

6. A circuit board having an electronic circuit formed thereon, the electronic circuit including a pair of multilayered ceramic capacitors, wherein each of the capacitors includes a body having dielectric layers formed of a dielectric ceramic material and internal electrode layers and a pair of external terminal electrodes formed on two sides of the body, the body being of a substantially hexahedral shape, the dielectric layers and the internal electrode layers being stacked alternately in the body and the internal electrode layers being connected in parallel to the external terminal electrodes in an alternate manner, characterized in that:

the capacitors are disposed at substantially plane-symmetrical positions on two opposite surfaces of the circuit board and substantially identical voltages are applied to the capacitors.

7. The circuit board of claim 6, wherein the capacitors are substantially identical each other.

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8. The circuit board of claim 7, wherein an electromechanical coupling coefficient of one of the capacitors ranges from about 70 to about 130% of that of the other capacitor.

9. The circuit board of claim 7, wherein a dielectric constant of one of the capacitors ranges from about 50 to about 150% of that of the other capacitor.

5 10. The circuit board of claim 7, wherein the number of layers of one of the capacitors is substantially identical to that of the other capacitor and a layer thickness of one of the capacitors ranges from about 70 to about 130% of that of the other capacitor.

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11. The circuit board of claim 7, wherein a layer thickness of one of the capacitors is substantially identical to that of the other capacitor and the number of layers of one of the capacitors ranges from about 70 to about 130% of that of the  
15 other capacitor.

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12. The circuit board of claim 7, wherein a length, a width and a height of one of the capacitors range from about 70 to about 130% of those of the other capacitor, respectively.

13. The circuit board of claim 6, wherein the capacitors are connected in parallel.

14. The circuit board of claim 6, wherein offsets between the  
25 capacitors are less than about 30% of a length and a width of one of the capacitors along the directions of the length and

the width, respectively.

15. The circuit board of claim 6, wherein an offset between center axes along length directions of the capacitors is less  
5 than 40 degree.

16. The circuit board of claim 6, wherein the electronic circuit is of a type in which voltages applied to the capacitors are varied.  
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17. The circuit board of claim 6, wherein the electronic circuit is a smoothing circuit of a power supply circuit and the capacitors are smoothing capacitors.

18. The circuit board of claim 6, wherein the electronic circuit is of a type in which voltages applied to the capacitors have frequencies varying in an audible frequency band.  
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19. The circuit board of claim 6, wherein the electronic circuit is of a type in which a voltage applied to one of the capacitors ranges from about 80 to about 120% of that applied to the other capacitor.  
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20. The circuit board of claim 6, wherein the electronic circuit is of a type in which an offset between phases of  
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voltages applied to the capacitors is less than about 20% of a phase period of a voltage applied to one of the capacitors.

21. The circuit board of claim 6, wherein the electronic  
5 circuit is of a type in which DC bias voltages are applied to the capacitors and a DC bias voltage applied to one of the capacitors ranges from about 80 to about 120% of that applied to the other capacitor.